BARC
NEWSLETTER

Contents

ANUPAM SUPERCOMPUTER SYSTEMS

H.K.Kaura, P.S.Dhekne, Sunita Mahajan, K. Rajesh, R.S. Mundada,
J.J. Kulkarni, B. S. Jagadeesh and D.D. Sonavane
Computer Division

The development of ANUPAM supercomputer systems based on parallel processing techniques has been the most outstanding achievement of Computer Division, BARC. ANUPAM Pentium III/16, is the latest and fastest supercomputer developed in April 2000, using 16 Pentium III @ 550 MHz. personal computers as compute nodes. This supercomputer is having a sustained speed of 3.5 Giga Flops, which is 2-3 times higher than the speed achieved on any of the supercomputers developed indigenously so far. In December 1991, Computer Division, BARC, entered the field of R&D in the supercomputing, when it developed the first supercomputer ANUPAM 860/4 using 4 Intel 860 microprocessor based boards as compute nodes giving a sustained speed of 30 Mega Flops. Subsequently, the computing speed available on the ANUPAM series of supercomputers was gradually increased by adding more number of compute nodes.
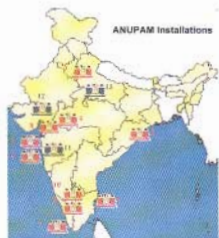
ANUPAM 860/64, a 64-node system, giving a sustained speed of 400 Mega Flops was operational in 1995. Presently, the ANUPAM-Alpha and ANUPAM-Pentium supercomputers using Alpha Workstations and Pentium Personal Computers (PC) as compute nodes, are being developed.

The supercomputers developed at BARC have proved to be highly reliable, highly cost effective, easy to use, easily up-gradable and also require much

less infrastructure for manufacturing. These supercomputers have been used extensively for solving many large compute intensive problems of BARC as well as many other R&D organisations in the country. Some of these problems were very vital for the success of R&D projects of national importance, and could not have been solved otherwise but for the availability of the ANUPAM supercomputers.

ANUPAM Installations

Present Installations
1. BARC, Mumbai
2. ITI, Mumbai
3. NCMRWF, New Delhi
4. CAT, Indore
5. IOP, Bhubaneswar
6. IGCAR, Kalpakkam
7. VSSC, Trivandrum
8. SRI Lanka(?), Trivandrum

Future Installations
9. IISc, Bangalore
10. ADA, Bangalore
11. NPC, Mumbai
12. Sch, Ahmedabad
13. IIT, Kanpur
14. UDCT, Mumbai

Fig.1 ANUPAM installations in India

The various models of ANUPAM-860 series of supercomputers are installed at BARC, Mumbai, IOP, Bhubaneshwar, CAT, Indore, IGCAR, Kalpakkam, and IIT, Mumbai. ANUPAM-Alpha series of supercomputers are installed at BARC, Mumbai, IIT, Mumbai, NCMRWF, New Delhi, and VSSC, Thiruvananthapuram. The latest Pentium-III based ANUPAM supercomputer installations are at BARC, Mumbai and ADA, Bangalore. Another Pentium based system has been recently set up at IOP, Bhubaneswar, while another 16-node ANUPAM-Pentium system at NPC is under installation. Similar systems are being planned at IIT, Kanpur, UDCT, Mumbai and also at VSSC,

Thiruvananthapuram. With the presently available parallel processing technology, the supercomputers based on Alpha workstations and Pentium PCs can be easily integrated up to 128 nodes thus giving a sustained speed of up to 25 Giga Flops on ANUPAM-Pentium and 50 Giga Flops on ANUPAM-Alpha series of super-computers. The systems are directly marketed through Technology Transfer & Collaboration Division of BARC. These can be procured by interested organizations either as complete systems or alternatively can be integrated on site with assistance from BARC, obtaining the required components, which are industry standard and available off-the-shelf, directly from the market and parallel processing software environment from BARC.

Background

High speed computing requirements have been growing exponentially for a large variety of

computational problems in science, engineering, defense, industry and business. It is well established that no R&D in the frontier areas of science and technology can be carried out without the support of high-speed computers. Due to sanctions, BARC has always been facing problems in procuring even ordinary high-speed computers for meeting its computational requirements. Also, conventional vector supercomputers were not easily available to other R&D and educational institutes in the country. Dual Cray X/MP was the only supercomputer that could be procured from USA by Department of Science & Technology (DST) for medium range weather forecasting, that too, after agreeing not to allow access to this supercomputer to any other organization. In view of the severe problems faced in procuring the supercomputers, Government of India initiated a mission mode project for development of supercomputer at Centre for Development of Advanced Computing (C-DAC), Pune in 1987 At the same time, another major effort in the development of supercomputing was initiated by Advanced Numerical Research and Analysis Group (ANURAG), Hyderabad, a Defence R&D Laboratory. Besides these two major efforts, National Aeronautical Laboratory (NAL), Bangalore, and Centre for Development of Telematics (C-DOT), Bangalore, also initiated R&D in the field of development of supercomputers. BARC initially decided to make use of the supercomputers developed by these organizations. However, various supercomputers developed by these organizations after an effort of 2-3 years were not able to meet the requirements of the scientific community at BARC. So it was decided to start our own R&D program in mid 1990. The approach followed at BARC was to concentrate R&D efforts only to the parallel computing aspects of the super-computing by making maximum use of the indigenously available off-the-shelf hardware and software components, rather than developing all the required components in BARC. As a result of this approach, the development cycle was considerably reduced thereby allowing the use of the latest available microprocessors giving highest speed/cost ratio. The first ANUPAM 860 supercomputer with four compute nodes was ready at BARC in December 1991, within six months of the initiating R&D. This was about 5 times faster than the other supercomputers available at that time in India delivering very high reliability with ease of usage at a significantly lower cost.

Parallel Processing Supercomputing Technology

Earlier during 1980s, the only type of super-computers available were conventional super-computers called "Vector Supercomputers" which achieved the supercomputing speed using the latest state-of-the-art electronic components for attaining highest feasible clock speed and advanced architectural features such as the very wide word, multi-stage pipelined execution of instructions and multiple arithmetic units. These supercomputers also had vector processing hardware units, consisting of a number of vector registers and floating point arithmetic units, which performed very high-speed computations on large vectors of floating point numbers. The cost of this type of supercomputers was enormous, as these computers contained very large amount of custom-built hardware, based on the cutting-edge electronic technologies, which generated large amount of heat and thus required sophisticated liquid cooling mechanism. Moreover, development of such supercomputers required huge amount of resources and highly skilled manpower, thereby limiting the design of such supercomputers in the hands of a few large manufacturers in the world.

Parallel Processing Supercomputers, on the other hand, make use of a number of readily available microprocessor based computers, concurrently working on various independently executable modules of a single computational problem, to attain the supercomputing speed. Since the speed available on microprocessors is increasing very rapidly, coupled with reduction of cost due to advances in VLSI technology, the parallel supercomputers provide highly cost effective alternative to the conventional Vector Super-

computers. Designing supercomputers based on parallel processing technology requires much less investment and also there is no theoretical limit on the speed achievable on such systems as is the case in conventional Vector Supercomputers. Development of parallel supercomputers has proceeded along two distinct trends. One of them involves high speed inter-connection of number of independent computing nodes, complete with their own memory and other resources, and software for synchronization and co-ordination of activities of compute nodes to achieve overall high speed of computation. These are the Distributed Memory Multiple Instruction Multiple Data systems. Other approach deals with connecting multiple processing units to multiple memory units through powerful interconnection architecture so that the entire memory is accessible to all the processors. This is the shared memory approach. Distributed memory systems can be built from the standard off-the-shelf components and besides having very low cost, they are also easily scalable whereas the shared memory systems are bogged down by the memory access bottleneck. This is the reason behind most parallel processing systems being distributed memory systems. ANUPAM series have followed the same distributed memory approach.

ANUPAM series of parallel processing super-computers consist of three major hardware components : master compute node, slave compute nodes and an interconnection network, and a parallel software environment. The master compute node carries out the overall control of the execution in parallel processing system and slave compute nodes carry out the execution of independently executable modules of a computational problem under the control of master compute node. The programmer divides a large computational problem into two independent program modules – master module which is loaded in master node, and slave module which is replicated in all the slave nodes. The data is partitioned in multiple domains to be executed concurrently in all the nodes. The master module

communicates with I/O, down-loads the data domains to the slave modules, controls the execution in a coordinated manner and collects the results from slave modules. They process the data sent by the master node and transmit back the result. The interconnection network provides the communication between master node and slave nodes. The overall speed of the Parallel Supercomputer depends upon the computing speed of the master node and slave nodes, computational load on each and communication efficiency. Since the speed available on micro-processors is increasing very rapidly, in order to achieve the maximum speed at the lowest cost and with the least number of nodes, the design cycle of the supercomputer should be very small or else, it would be obsolete before it started.

The interconnection network is the next most vital component of the Parallel Processing Super-computer. There are a number of approaches possible for high-speed interconnection network. For shared memory systems, it could connect processor modules with the memory modules. The interconnection network can be a bus, a crossbar switch or a multistage interconnection (MIN) switch. The MIN and crossbar switches are complex to manufacture. The bus has latency problem and memory access bottleneck. In distributed memory systems, the interconnection network consists of a bus, multiple busses, hypercube, or a switch. It should have a very high speed of communication, be easy to interface and it should also have low latency. Communication speed between any two nodes should be uniform across the system. Shared memory inter-connection networks are specialized pieces of hardware and hence difficult to procure. Distributed memory systems can be connected by same communication hardware like Ethernet used for LANs and ATM used for WANs. This leads to vendor independence and assurance of getting the fastest switches as they enter the market. All these aspects were considered in designing the different versions of ANUPAM series.

ANUPAM Series of Supercomputer Systems

Initially, Computer Division, BARC, developed ANUPAM 860 series of supercomputers which used processor boards based on Intel i860 microprocessors as compute nodes and multiple busses, i.e. Multibus-II and modified wide SCSI, for inter-processor communication. Since 1997, ANUPAM Alpha and ANUPAM Pentium series of supercomputers are being developed based on industry standard high-speed network switches and either Alpha Server/Workstations or Pentium Servers/ PCs as compute nodes. Very high-speed inter-processor communication is provided by one of the high-speed switches like ATM, fast Ethernet and Gigabit Ethernet. One of the major bottlenecks found in most parallel processing architectures is the I/O handling. On ANUPAM, this lacuna has been removed by providing dedicated file servers having two independent high speed networks, one for handling file systems via network file system (NFS) and the other for inter-process communication.

ANUPAM-860

First ANUPAM-860/4 was developed in December 1991. It made use of Intel i860 microprocessor @ 40 MHz, based mini computers as master nodes

ANUPAM-860 64-node

Sustained speed on 64 nodes :- 400 Mflop
Year of introduction :- 1995

Fig. 2 ANUPAM-860 system

and 4 Intel i860 based processor boards with on-board memory as compute nodes all in one chassis. Each compute node had a peak speed of 80 Mega Flops. These compute nodes were interconnected using industry-standard Multibus-II back-plane bus of the mini computer, which provided a uniform communication speed of 40 MBytes/sec between any two compute nodes of the system. The overall sustained speed of the system for user jobs was 30 Mega Flops. The system was later on upgraded to 8 nodes in August 1992 giving a sustained computational speed of 52 Mega Flops. This involved redesigning of the processor boards so that 8 slave compute nodes could be accommodated in the same single 860 mini computer multibus-II chassis. The system was further upgraded to 16-node ANUPAM-860 in November 1992, giving a sustained speed of 110 Mega Flops. This involved coupling of two 860 mini computer chassis with the wide SCSI interface, developed specially for Multibus-to-Multibus communication. This provided a communication speed of 20 Megabytes per second. Subsequently, ANUPAM 860/32, a 32-node system was developed in February 1994 by interconnecting 4 mini computers Multibus chassis, using the multiple wide SCSI busses. The system was further upgraded to 64 nodes in November 1995 by adding 32 more slave compute nodes which were designed using the latest Intel 860 microprocessor @ 50 MHz and providing up to 256 MB on board memory. The 64-node ANUPAM-860, gave a sustained computational speed of 400 Mega Flops, which was equivalent to the speed of CRAY Y/MP Vector Supercomputer.

ANUPAM-Alpha

First of ANUPAM-Alpha series of supercomputers was developed in July 1997 giving a sustained speed of 1000 Mega Flops on 6 compute nodes. This system made use of six Alpha servers, based on Alpha 21164 microprocessor @ 400 MHz as node processors and Asynchronous Transmission Mode (ATM) switch operating at a peak speed of
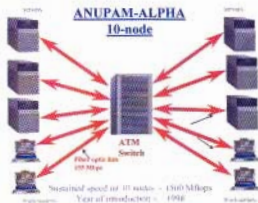
Fig. 3 ANUPAM-Alpha system

155 Mbps and sustained speed of 134 Mbps as interconnecting network. The design of the system differed significantly from the earlier ANUPAM-860 design. This system used complete servers/ workstations with memory, disk, other I/O and operating systems as compute nodes instead of processor boards with only memory as compute nodes in the earlier ANUPAM-860 series of systems. This permitted disk I/O on slave compute nodes, use of any node as master node and simultaneous processing of a mix of sequential and parallel jobs, resulting in a very high utilization of the entire hardware. The system was further upgraded to ANUPAM-Alpha/10 in March 1998 by adding 4 compute nodes, thus giving a sustained speed of 1.5 Giga Flops on 10 nodes. ANUPAM-Alpha series of supercomputer can be easily upgraded to 128 nodes, thus giving a sustained speed of about 50 Giga Flops using currently available Alpha 21264 microprocessors @ 700 MHz.

Another ANUPAM-Alpha/8 system was developed for National Centre for Medium Range Weather Forecasting (NCMRWF), New Delhi, in September 1999. The system made use of 2 Alpha servers and 8 Alpha workstations based on Alpha 21164 microprocessor @ 600 MHz as compute nodes and two Gigabit Ethernet switches for inter-communication. The system was configured as 2 identical systems with 1+4 node configuration each

to provide full redundancy for highly reliable operation required for the production run of medium range weather forecasting computations. The entire system runs at 3 Giga Flops speed.

One more ANUPAM-Alpha system has been installed at Vikram Sarabhai Space Centre(VSSC) at Thiruvananthapuram. VSSC has been actively involved in solving highly complex Computational Fluid Dynamics (CFD) equations for computing turbulent liquid flow. Since May 1998, they have obtained a set of 8 Dec Alpha workstations at 500 MHz speed, each having 512 MB memory. The whole set of workstations is connected via fast Ethernet switch. VSSC scientists have parallelized their CFD applications using the standard message passing library MPI on the network of Dec Alpha workstations. CFD programs are highly compute-intensive but fortunately extremely parallelizable. When VSSC scientists visited BARC, they ran benchmark programs using both MPI and ANULIB calls and were happy with the gain in performance with ANULIB.

ANULIB also gives better performance than another message-passing standard PVM. This was benchmarked at our center. The ANULIB/PVM comparison which has been done for Linpack benchmark is given below:

No of CPUs	ANULIB	PVM
1	45.13	45.13
2	89.55	81.3
3	133.44	116.3
4	177.15	144.0
5	220.1	167.9
6	260.5	185.7
7	280.5	196.7
8	301.7	204.7
9	321.0	213.1
10	342.9	220.0

MFLOPS rating for Linpack
(1000*1000) double-precision matrix

The main attraction of this system comes from ANULIB which is faster and compatible to the older version of ANUPAM, thus offering upward compatibility to the ANULIB users.

ANUPAM-Pentium

ANUPAM-Pentium PIII

16-node

Giga for Ethernet Switch

16 Pentium III, 550 MHz, Personal Computers

Display Monitor

Installed Speed of 16 nodes   - 3.5 Giga flops
Expandability   - 128 Nodes
Estimated Speed on 128 nodes   - 25Giga Flops
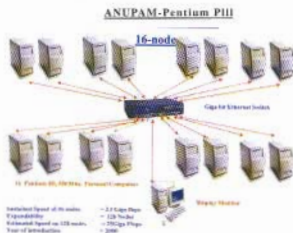Year of Introduction   - 2000

Fig.4 ANUPAM-Pentium system

The computing speed available on personal computers based on the latest Pentium Microprocessors have increased to a level almost matching the speed of workstations based on RISC microprocessors and they also support large RAM memories required for large compute-bound jobs. Being commodity items, these personal computers are readily available at much lower prices from multiple vendors. The development work on ANUPAM-Pentium series of supercomputers based on Pentium PCs was initiated in January 1998, the main focus of development being minimization of cost and the targeted enduser being from Academia and Universities, who should have a parallel machine at affordable cost. The first ANUPAM- Pentium II/4 using 4 Pentium II PCs operating @ 266 MHz as compute nodes and a fast 100 Mbps Ethernet switch for interconnection was ready in July 1998. This gave a sustained speed of 248 MFlops. Subsequently ANUPAM-Pentium II was expanded in March 1999 to 16 nodes using Pentium II personal computers @ 330 MHz giving a sustained speed of 1.3 Giga Flops. In April 2000, the system was further upgraded to Pentium III/16 using 16 Pentium III personal computers @ 550 MHz as compute

nodes and a Gigabit Ethernet switch for interconnection, giving a sustained speed of 3.5 Giga Flops. This is the fastest supercomputer operating in the country having a speed of 2-3 times faster than any other available computer. ANUPAM-Pentium series of supercomputers can be easily upgraded to 128 nodes for meeting any desired speed requirement up to 25 Giga Flops.

Another major achievement was the ANUPAM PIII system installed at Aeronautical Development Agency (ADA), Bangalore in June 2000. The ANUPAM system at ADA gives 5 Giga Flops speed for their CFD code VASBI. The parallel system has 16 compute nodes and a file server. Each node has a Pentium-III @ 550 MHz, with 256 MB memory and 16 hard disk. The file server is also Pentium-III @550 MHz, with 512 MB main memory and 40 GB hard disk. The nodes and file server are interconnected by a Fast Ethernet switch of 100 Mbps speed.

ANUPAM Software Environment

Developing a program for execution on a parallel processing system is a much more difficult process than doing the same on a sequential computer. The parallel program has to be partitioned into multiple independently executable tasks that can be executed concurrently on multiple nodes, thereby gaining high computational speed. The software environment should co-ordinate overall execution of the parallel system, balance the load on all the nodes and provide tools for parallelising and debugging users programs.

ANUPAM computer systems are based on Multiple Instruction Multiple Data (MIMD) distributed memory architecture, with each node having its own local memory. It is a No Remote Memory Access (NORMA) architecture. The programs in each system execute independently, communicating explicitly through message passing between the nodes. ANUPAM series' programming model is the Master/Slave model where the main portion of the program executes in a compute node which is called master node, and the other parts

execute in other compute nodes called slave nodes, under the control of Master and Slave tasks. The function of the master task is to partition data in different domains, to transfer the slave domains to slave compute nodes and to execute its own domain. The master task then controls the execution of slaves, collects the result from the slaves and performs input/output operations. The slave tasks accept their portion of program and data domains, execute them and pass the results to the master task. The communication between the tasks is carried out explicitly via communicating network through messages. The message passing is implemented as a set of library routines providing calls for sending/receiving data as a single element or as buffers. Due to the architectural differences between ANUPAM-860 and other ANUPAM series, the software environment for the slave nodes varies for ANUPAM-Alpha and ANUPAM-Pentium series, though the user interface of ANULIB – the message-passing library remains exactly identical, providing upward compatibility.

Software Environment on ANUPAM-860

In the ANUPAM-860 series of systems, the operating system and other system software like C and Fortran, Compilers, Vectoriser and Debugging aides, etc. reside only in master node. The slave nodes do not have the standard O.S. and compilers, and are controlled by a monitor program developed as a part of system software. The parallel processing software for ANUPAM-860 was developed at two levels - System level and Application level. System level software consists of writing the control program for slave nodes, which includes an absolute loader and an error handling routine for floating point exceptions occurring in the slave nodes, a stripper program and a down loader for master node and message passing run time library for master and slave nodes with the relevant device drivers, added to the software component. Application level software consists of various parallel program development tools like –

- ANULIB - the message passing library

- PSIM - the simulator for ANULIB which provides the same user interface as ANULIB and runs on a sequential machine. It proved to be extremely useful in developing user programs which could run on single systems during initial debugging stages, thus saving the parallel machine for production runs.
- S-Trace and PSIM-Trace - utility for tracing run-time error
- PSHED - utility for semiautomatic parallelization
- FPROF - a sequential profiler
- FFLOW – a Fortran-flow analyzer
- FDB –PFDB – debuggers for sequential and parallel programs

Moreover, user level parallel libraries like SCLIB-numerical library, IMAGEPRO- parallel image processing applications and XMOL, XIMAGE – scientific visualization packages are developed.

Software Environment on ANUPAM Alpha and ANUPAM Pentium series

ANUPAM-Alpha and ANUPAM-Pentium series of computer systems have identical software environment on each node. Operating system, C, Fortran compilers and debugging aides form the standard system component. Since both the interconnection networks, ATM and Ethernet, use TCP/IP, the message-passing library ANULIB has been implemented on TCP/IP using socket library calls. This gives architectural independence as well as network independence. ANULIB can be implemented on any system offering socket library interface. The present environment facilitates multiple parallel programs execution; disk I/O on all nodes and flexibility of choosing any of the nodes as master node. Similarly, PSIM is available as a mode of operation where all nodes are mapped on a single node. All program development tools of ANUPAM 860 are also present. Additional utilities like SYN- syntax checker and ANULIB-to-MPI converter have been provided. There is a file server, which holds the entire user accounts, and they are shared through Network Information Service (NIS). Network File System (NFS) is used to share all the user files. Another utility is auto-

mount daemon, which automatically mounts remote directories requested by the user. The combination of NIS, NFS and automount make all the systems appear identical to the user and parallel programs can be submitted from any system. A special facility called 'Hold' has been developed to halt the entire parallel program execution for a certain period and then continuing from the same point of execution.

ANULIB is the message-passing library, developed for both C and Fortran languages. It is a tool for explicit parallelisation, which is implemented through message passing, involving a set of send/receive calls. ANULIB has 4 modules:

- Module 1 – initialization and termination calls for master and slave programs,
- Module 2 – communication of messages for transfer of a single element, multiple elements and buffers and broadcast to all nodes.
- Module 3 – error handling module,
- Module 4 – ANUSER daemon for execution of slave programs.

Other parallel libraries such as PVM (Parallel Virtual Machine) and MPI (Message Passing Interface) are also implemented on the ANUPAM system. However, the performance with the ANULIB is 20-30% better than the other libraries.

Applications

For using parallel supercomputers, considerable effort is involved on the part of program developer, since large programs normally developed for conventional sequential computer require modifications before they can be executed on parallel supercomputer. Thus, necessary conditions for the use of the parallel computer are the availability of the source code, possibility to divide the program into fairly independently executable modules and minimum communication between the concurrent modules. Thus, for minimizing the required parallelization effort, many advanced tools for parallelisation, debugging, profiling, load balancing and optimizing should be provided. ANUPAM-series of supercomputers, besides being

very fast, easy to use, highly reliable and cost effective, are very rich in terms of parallelising tools as compared to other available parallel supercomputers.

All the three series of supercomputers – ANUPAM-860, ANUPAM-Alpha and ANUPAM-Pentium – have been extensively used for solving some of the very large computational problems for BARC. ANUPAM systems have also been used by many other R&D organizations in the country. Replacement of CRAY X/MP supercomputer at NCMRWF, Delhi, for running operational weather forecasting codes with ANUPAM-Alpha, and the recent installation of ANUPAM-Pentium at ADA, Banglore, for CFD computations related to aircraft design, have been two most significant achievements of national importance of ANUPAM systems in supercomputing.

Applications at BARC

BARC has used ANUPAM series of super-computers for the past ten years for solving large computational problems in various frontier fields of science and engineering. Some of the major applications implemented on ANUPAM super-computers are as follows: -

1. *Molecular Dynamics Simulation :* This simulation is carried out by setting up a box consisting of a number of particles. Then, assuming certain starting values of positions and velocities of atoms, the equations of motion are solved iteratively with a small time step, with the new iteration utilizing the results of the previous cycle. The parallelization is done on calculating the net forces on the atom at each time step and the values of atomic coordinates are passed between processors for each iteration. This involves minimum communication and can be scaled very nicely with more number of nodes.

2. *Crystal Structure Analysis :* In this problem, computations are required for the processing and analysis of huge experimental data, optimising thousands of structural parameters and visualisation of 3 dimensional structures of
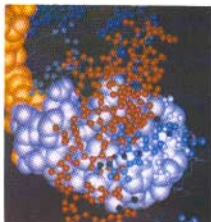
Fig. 5 Protein molecule structure

biological macromolecule like Proteins. It has been parallelized using data domain partitioning technique. Data partitions are totally independent leading to very little inter process message passing. It is a very scalable algorithm using event parallelism.

3. Neutron Transport Calculations : This problem involves solving of neutron transport problems, involving complicated geometry and large flux gradients using Monte Carlo method. A large amount of computations is needed for reducing uncertainties associated with this method by increasing number of histories. Since the individual histories are essentially independent, this is a good example of event parallelism.

4. Gamma Ray Simulation by Monte Carlo Method: This simulates the development of the electromagnetic cascade, initiated by Cosmic Gamma ray, in the earth's atmosphere. This simulation enables one to device and tune the performance of the detector for the detection of Cosmic Gamma Rays from extra-terrestrial source.

5. Three Dimensional Electromagnetic Plasma Simulation : This simulation demands high performance computers and are used for studying plasmas of various types such as those occurring in high power microwave cavities, magnetic confinement fusion devices and in earth's magnetic sphere. Parallelization has considerably reduced
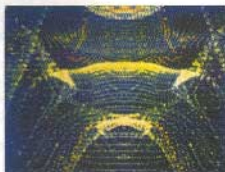
Fig. 6 Electromagnetic plasma simulation

the time taken to analyze and display various time frames of electromagnetic plasma.

6. First Principle Electronic Structure Computations : These are used for computing inter-particle potentials at various ionic configurations for finding new materials and predicting their behaviour under static and dynamic pressure. These calculations make heavy demand on computation speed, for even a medium sized sample containing 10 to 100 atoms. This is an example of fine grain parallelism where data is exchanged at every iterative loop.

7. Finite Element Analysis Method : Finite Element Analysis program for carrying out linear static and dynamic analysis of arbitrarily loaded axisymmetric plates and shells requiring large amount of computations has been implemented. The shell may be meridian curve of any shape.

Structure Analysis

Fig. 7 Structure Analysis

8. *Laser-Atom Interaction Computation* : Computation of intense field Laser-Atom interaction is a very complex problem. In recent years, there is an intense activity in the direct solutions of Schrodinger equation (SE) involving time dependent (TD) interactions. This necessitates high performance computing solutions. This program has been successfully on ANUPAM parallel system.

Applications in Outside Organizations

1. *Weather Forecasting at National Centre for Medium Range Weather Forecasting (NCMRWF), Delhi* : Dual CRAY X/MP Supercomputer, procured in 1988, was being used for Medium Range Weather Forecasting at NCMRWF, Delhi. The search for the replacement of this supercomputer was started by Department of Science and Technology in 1994. Since procuring such a computer from abroad involved difficulties due to technology control regime and since various

Weather Forecasting

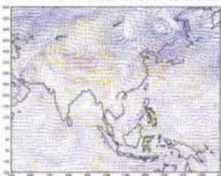850hPa WIND&OP-NCMRWF MODEL-T80 24HR FCST ANUPAM-ALPHA

Fig. 8 Medium Range Weather Forecasting Model

organisations in the country were actively involved in developing supercomputers, it was decided to attempt the replacement of the Cray with the indigenous product. The job involved porting of entire suite of weather forecasting programs, primarily consisting of Modeling Code T-80 and Analysis Code SSI, from CRAY supercomputer to the parallel supercomputer developed locally. Since CRAY is a 64 bit computer and many of the

routines were written in assembly language of CRAY, the first challenge involved re-writing of fresh routines, replacing many of CRAY specific functions and libraries, and obtaining the Weather Forecasting Results with the same accuracy as achieved on CRAY. The second challenge was to parallelise the codes on the local supercomputers so that the time taken for the complete execution of the weather forecasting suite is less than the time of execution on CRAY.

So far, out of all the indigenously developed supercomputers, only ANUPAM-Alpha with (1+4) one master and four slave node configuration, has been able to meet both the conditions of matching accuracy and execution time on CRAY. An ANUPAM-Alpha system was fully commissioned at NCMRWF, Delhi, in December 1999, thus providing a solution to a long-standing problem of finding an alternative to obsolete Dual CRAY X/MP supercomputer. The ANUPAM system, having fully redundant configuration for the very high availability required for the production run, is operating very satisfactorily for the past several months. This has resulted in saving the huge maintenance expenditure on obsolete CRAY system and eliminated dependence on it for medium range weather forecasting applications. ANUPAM-Alpha system, using Alpha 21164 @ 600 MHz microprocessor based workstations, can be easily upgraded to provide a 2.5 times faster computational speed by using the latest available workstations, based on Alpha 21264 microprocessor.

2. *Computational Fluid Dynamics, Aeronautical Development Agency (ADA), Bangalore* : Solving Computational Fluid Dynamics problem for studying airflow through air-intake ducts of an aircraft is one of the very large computational problem demanding huge amount of computations. This problem became one of the major challenges to the indigenously developed supercomputers. VASBI, a three dimensional explicit finite volume code in computational fluid dynamics, was developed at ADA. VASBI code obtained the compressible turbulent viscous flow through

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symmetric bifurcated air-intake ducts by solving the 3-D unsteady Reynolds averaged Navier-stokes equations. This code was taking 30 days of computation for a single result on the fastest sequential computer available at ADA. It was implemented on ANUPAM-860 in 1994 giving one result in less than 2 days. Thus, this challenging problem was solved using the ANUPAM-860 system for a dedicated period of 2-3 months.
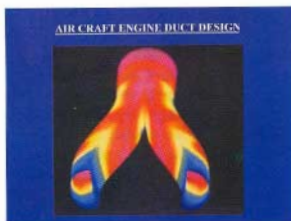

Fig. 9 Air craft engine duct pressure diagram

Recently ADA had another problem of Computational Fluid Dynamics involving 4 million grid points. This problem could not even be loaded on any of the supercomputers available in the country. It was implemented on a 16-node ANUPAM-Pentium II developed last year using 16 Pentium-II PCs with 760 MB memory each. Based on the benchmarking and evaluation carried out on ANUPAM-Pentium supercomputer, ADA decided to procure this system from BARC. An ANUPAM-Pentium based on the latest Pentium III PCs was installed at CFD Labs, ADA on June 1, 2000. This system is 5 times faster than the existing PACE-32 supercomputer at ADA, supplied by ANURAG, Hyderabad, at a cost of Rs. 2 crores. ANUPAM supercomputer at ADA has 16 nodes and a file server; each node is Pentium III PC @ 550 MHz with 256 MB memory each. The file server and the nodes are interconnected using Fast 100 Mbps Ethernet Switch. The cost of the system is Rs.30 lakhs. Most of the industry standard components such as PCs and Ethernet Switch were procured directly by ADA. The ANUPAM parallel system

was integrated at site by a team of three experts from BARC in a period of less than a week. ANUPAM-16, being the fastest system available at ADA, would be used for solving many new large CFD problems. This can be easily upgraded to higher configuration for undertaking even larger problems in future.

The list of ANUPAM installations in the country is given below:

Existing Installations

1. BARC, Mumbai
2. IIT, Mumbai
3. NCMRWF, New Delhi
4. CAT, Indore
5. IOP, Bhubaneshwar
6. IGCAR, Kalpakkam
7. VSSC, Thiruvananthapuram
8. MS University, Vadodara
9. IISc, Bangalore
10. ADA, Bangalore

Proposed Future Installations

11. NPC, Mumbai
12. IIT, Kanpur
13. UDCT, Mumbai

Conclusion

R&D in the field of developing parallel super-computers, undertaken at BARC for the past ten years, has been very successful in meeting the supercomputing requirements of BARC and other R & D organisations in the country. ANUPAM super-computers developed at BARC have features of very high speed, high reliability of operation, ease of usage and are highly cost effective. Using this technology, the design cycle of the system has also come down very significantly. Thus, the supercomputer based on the latest micro-processors can be integrated within a short period of 1-2 weeks of procuring the required components, thereby, giving the best possible speed on minimum number of compute nodes in a most cost effective manner. ANUPAM supercomputers are

very easy to manufacture as the components used are industry-standard readily available at competitive cost. ANUPAM systems can be integrated at site by obtaining the components directly from market and procuring only the parallel processing hardware and software environment from BARC. With the presently available components, the system with sustained computational speeds up to 50 Giga Flops can be easily integrated which is matching the computational speed available on any of the supercomputers available abroad.

INTEGRATED GARTER SPRING REPOSITIONING SYSTEM (INGRES) FOR REMOTE REPOSITIONING OF GARTER SPRING SPACERS IN COOLANT CHANNELS OF 220 MWe PHWRS

B.S.V.G. Sharma and B.B. Rupani
Reactor Engineering Division

Introduction

Garter spring (GS) spacers maintain the spacing between the Pressure Tube (PT) and the Calandria Tube (CT) of Pressurised Heavy Water Reactor (PHWR) coolant channels. The actual location of GS spacers in PHWR coolant channel plays very significant role in maintaining stipulated service life of coolant channels. The displaced GS spacers can lead to develop contact between the PT and CT resulting in formation of hydride blisters over a period of operation. The embrittlement and cracks caused by the hydrides (developed in the form of blisters) will result in rupture and will lead in eventual failure of PT.

There has been evidence of these GS spacers shifting from their installed locations in the early generation Indian PHWRs. Hence, there was a need to design and develop a tool which can precisely detect and reposition these displaced GS spacers in the PHWR coolant channel assembly. The INtegrated Garter spring REpositioning System, abbreviated as INGRES, has been designed and developed for repositioning the GS spacers in the highly radioactive coolant channels of 220 MWe PHWRs. The tool can be operated remotely from control room located at a distance of 100 meters (cable distance) from reactor vault to minimise radiation exposure of operating personnel.

Fig.1 INGRES-2S system under operation at MAPS-1

The INGRES system consists of eddy current transducers, linear induction motor and bending modules assembled as integrated tool along with auxiliary support equipment for remote detection and repositioning of GS spacers in the PHWR coolant channel assembly. The auxiliary support system equipment consists of INGRES tool carrier cum delivery system, variable frequency power

supplies, hydraulic and pneumatic pumps, main, auxiliary and interfacing control panels for the control and operation of the tool.

The first version of the tool (version INGRES-1S) was developed in the year 1995. This tool needed both the fueling machine vaults of PHWR for its operation. Subsequently, the next version of tool namely INGRES-2S was developed in the year 1997 for single vault operation. Both these systems are meant for dry channel operation.

This report describes general features of the hardware modules, control and automation software modules and support equipment of the system. The INGRES-2S system has been successfully used for repositioning garter spring spacers in Madras Atomic Power Station (MAPS) unit-1 during March-April 2000 (Fig 1). It has extended the life of 28 coolant channels of the said reactor by 1.5 effective full power years (approximately 3 calendar years). The rehabilitation of coolant channels of MAPS-1 is also highlighted in this report.

Design Philosophy and Constraints in Development of INGRES

The GS spacers are not physically accessible from either side of coolant channel as they are concealed/confined in the annular space between PT and CT of coolant channels. The schematic view of PHWR coolant channel assembly showing PT, CT and GS spacers is shown in Fig. 2. The only access available to the repositioning tool for repositioning these spacers will be its insertion through the inside of pressure tube (Fig. 3).

One way of imparting physical movement in GS spacers for repositioning will be by generating mechanical force in it by means of electromagnetic induction technique. The interaction between primary and secondary electromagnetic fields (that are generated by primary device and produced in GS spacer circuit by induction respectively) will cause the movement of unpinched GS spacers.
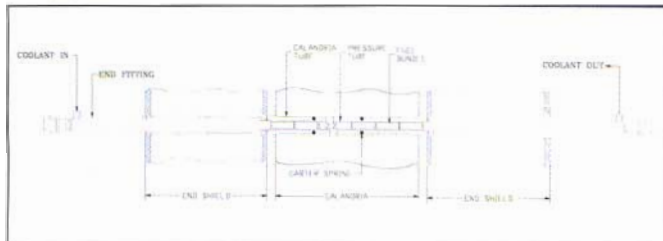

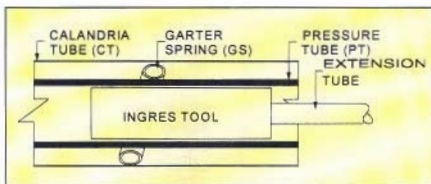Fig. 2 PHWR coolant channel assembly schematic

Fig. 3 INGRES tool in coolant channel

As such the tool should have transducers for precise detection of GS spacers and PT-CT eccentricity. It should have electromagnetic device to produce physical force on GS spacers by electromagnetic induction to move them in axial direction. Further, there should be pressure tube bending or flexing tool for correcting their eccentricity at the GS location to unpinch the spacers to facilitate their movement. In addition to these basic modules, the system should have auxiliary support systems to position and control the tool operation in the coolant channel.

There are various constraints on the design, size and operating parameters for the tool. These are described below:

(a) Physical In-accessibility of GS spacers
(b) Hostile operating conditions, viz. operation under intense radiation fields and presence of heavy water in channels during tool operation.
(c) Pinched condition of GS spacers makes it difficult to move unless they are unpinched.
(d) Unfavourable electrical and magnetic properties of the PT, CT and GS spacers. They are made of zircaloy.
(e) Shielding effect of pressure tube is unfavourable for force generation in garter spring spacers by electromagnetic induction device. This affects repositioning of GS spacers.
(f) Presence of muck in annulus region of PT and CT, distortion in shape of GS spacers and electrical contact resistance of girdle wire play

significant negative role during GS repositioning operation.
(g) Requirement of smaller size and weight of tool. The tool diameter should not exceed 80mm and none of the modules of the integrated tool should exceed length of fuel bundle (around 500mm). Suitable universal couplings should be used between modules.
(h) The tool should have features like moderate operating voltages, remote operability from control room and reasonable in-channel service life during operation.

Major Modules and Essential Features of INGRES

The INGRES-2S tool head is shown in Fig.4A and 4B. Fig.5A shows the schematic of INGRES-2S setup in reactor fuelling machine vault and Fig.5B shows schematic of auxiliary and support equipment of INGRES-2S.

The work involved was indigenous design and development of following modules of the system.

1. A transducer system for precise detection of garter spring spacers in PHWR coolant channels, under elevated operating temperatures (90 to 95 Degree C). The **GSDP (Garter Spring Detection Probe)** eddy current transducer system has been developed for precise detection of GS spacers as per requirements.
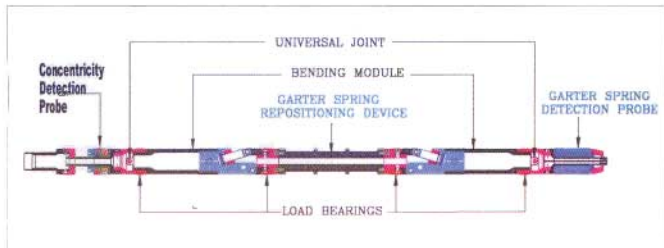

Fig 4A INGRES-2S tool head

INGRES-2S TOOL

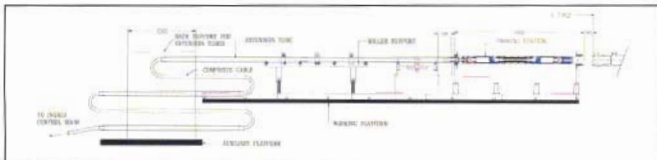Fig. 4B INGRES-2S tool head

Fig. 5A Schematic of INGRES-2S setup in reactor F/M vault
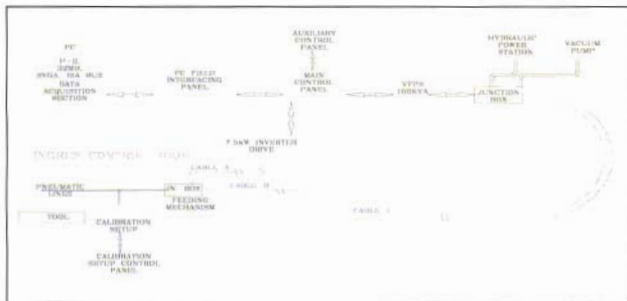

Fig. 5B Schematic of auxiliary equipment of INGRES-2S system

2. A transducer system for Qualitative & Quantitative detection of PT-CT eccentricity : This information is essential to plan un-pinching operation of GS by actuating Bending Module of the system. The **CDP (Concentricity Detection Probe)** eddy current transducer system has been developed for precise detection of PT-CT eccentricity within an overall accuracy of +/-1 mm.

3. A compact electromagnetic device working on moderate operating voltage (415V 3 Phase AC) to induce electro-mechanical force on GS spacers by linear induction principle to facilitate their movement. The **GSRD (Garter Spring Repositioning Device)** is a non-conventional tubular linear induction motor which has been designed and developed for generating intense electromagnetic field in the vicinity of GS. This induces current in the girdle wire of GS by induction. The flux generated due to girdle wire current opposes the main flux of GSRD creating mechanical force on the GS spacers resulting in its movement.

4. A Device for flexing the Pressure Tube to correct PT-CT eccentricity to facilitate unpinching of GS spacers. The BM (Bending Modules: 2 Numbers), namely forward and rear bending modules, have been designed and developed to flex the pressure tube in desired direction to correct their eccentricity and hence to unpinch the GS spacers. These devices are actuated hydraulically, which can be precisely controlled to adjust the lift of PT relative to CT for perfect unpinching of GS spacers.

5. A PC based control system for precise control of tool operation. A PC based control system namely INGRES-2S control version 2VB has been developed. The user software and control hardware for the system has been designed and developed using Visual Basic version 5.0 and other associated software. The software is having exclusive features for auto detection of GS spacers and tool positioning functions with audio visual feedback to the operator.

Necessary safety interlocks have been incorporated in the control system for safe operation of tool in the reactor channels. Fig.6 shows typical view of PC screen showing features of the custom made software developed and used for the control and automation of the system.

6. Tool carrier and positioning mechanism : Electro-pneumatic tool positioning mechanism has been developed for precise positioning of tool in the reactor coolant channels.

7. Umbilical cable : A special umbilical cable has been developed which contains hydraulic and pneumatic hoses, instrumentation, thermo-couple extension and electrical power cables needed for controlling the operation of various modules of INGRES tool remotely from a distance of 100 meters from the tool head.
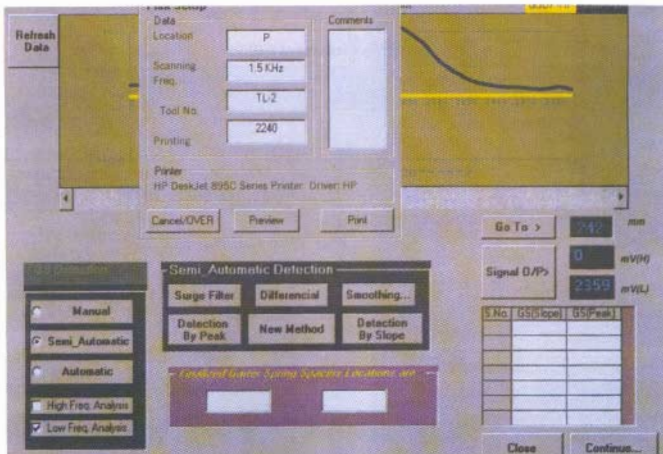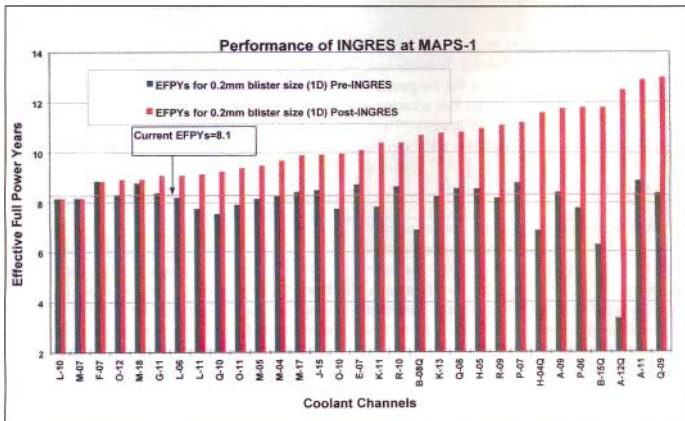

Fig. 6 INGRES control software features

Fig. 7 Life extension of MAPS-1 coolant channels by INGRES-2S

Table 1: Unique features of INGRES

Parameter	Features
ID of Pressure Tube	83 mm*
Gap between Pressure Tube (PT) & Calandria Tube (CT)	8.5 mm
Diameter of Garter Spring (GS)	6.8 mm
Eccentricity between PT &CT	Exists*
Gap for maneuvering the Concentricity	1.7 mm*
Repositioning Criteria	Optimum Location of GS
Nos. of Garter Springs	2*
Condition of Channel	Dry (Tool designed & tested for Wet Channel)
Cost of Disposable Tool	Rs.4 Lakhs
Developmental Cost	Rs.110 Lakhs
Maximum Movement per Firing	145 mm
Demonstrated Life of Tool inside Core	353 Hrs (still functioning)
Average Time for Repositioning	10 Hrs per Channel
Time for Installation of System	48 hours for Parking Station

" * "⇒ Challenging parameters

8. Control panels : The operation of tool is controlled through various control panels. The control circuits are so designed that it can operate the INGRES tool through PC in auto mode of operation. During emergency or at the time of PC failure, the manual intervention is possible by selecting manual mode operation.

9. Auxiliary equipment: The system uses special power supplies and hydraulic and pneumatic systems. These systems have been procured and incorporated.

Rehabilitation of Coolant Channels in MAPS Unit-1 by INGRES-2S

During April 2000, INGRES-2S has been successfully used for repositioning garter spring spacers in coolant channels of MAPS-1. The life of 28 coolant channels has been extended by 1.5 effective full power years (approx. 3 calendar years). Fig. 7 shows performance of INGRES-2S tool in MAPS-1.

Conclusion

INGRES system has been developed in Reactor Engineering Division (RED) of BARC for predicting and extending safe operating life of coolant channels of early generation Indian Pressurised Heavy Water Reactors (PHWRs), with loose fit garter springs vulnerable to shifting from their installed positions. INGRES is used to remotely move the inaccessible garter springs in the annular gap between calandria tube and pressure tube to desired axial position. INGRES incorporates indigenously developed sophisticated electrical, electronics, instrumentation, pneumatic, hydraulic and mechanical subsystems. The system is operated through computer interface located in a special control room outside the reactor building.

On account of the compactness of the Indian 220 MWe coolant channel, the challenge for design & development of INGRES has been very large. The unique features of INGRES system are highlighted in Table-1. Presently RED, BARC, is working for development of wet version of the system to save the reactor down time.

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RUSSIAN PRESIDENT VISITS BARC

Russian President Mr Vladimir Putin visited BARC on October 5, 2000. He is the first leader of Russia to visit BARC.

Mr Putin visited Dhruva reactor and also an exhibition specially put up for the occasion depicting the scientific and technological strength of the Department of Atomic Energy.

Russian President Mr Vladimir Putin being taken to the Central Complex Auditorium for an exhibition at BARC.

While addressing the gathering of senior scientists of DAE, Mr Putin lauded the achievements of DAE and complimented them for their accomplishments. He said that he was impressed by the Indian reactor safety record. He described BARC as a 'temple of science and technology of the 21st century'. The President also remarked that the interaction between India and Russia on peaceful uses of atomic energy dates back to early 1970's and it continues till date.

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SEMINAR IN HINDI ON RADIATION AT TARAPUR

A Seminar in Radiation was organised on December 15, 2000 by the Official Language Implementation Committee, BARC, Tarapur. The Seminar was inaugurated by Mr A.M. Meghal, Uranium Extraction Division, BARC, who also presided over the function. Nearly 110 persons participated in the Seminar. The following persons delivered lectures during the Seminar :

Mr H.S. Sukheswala, Atomic Energy Regulatory Board, Mumbai, on "Natural and Artificial Source of Radiation and Safety"; Dr Sharad Pawar, Nuclear Agriculture & Bio-Technology Division, BARC, on "Contribution of Radiation in the field of Agriculture"; Dr V. Rangrajan, Radiation Medicine Centre, Parel, Mumbai, on "Radiation in Diagnosis and Treatment of Diseases"; Mr D. Mitra, Isotope Division, BARC, on "Contribution of Radiation in the field of Industrial Progress"; and Dr Brij Bhushan, Food Technology Division, BARC,on "Preservation of Food Items by Radiation."

Seminar on Radiation organised by the Official Language Implementation Committee, BARC, Tarapur. (Left to Right) : Mr D. Mitra, Dr Brij Bhushan, Dr Sharad Pawar; Committee Members : Mr Nandkumar L. Sonar; Mr Kaushal Kumar Srivastava, Mr Ramharakh R. Singh, Mr Amrut Prakash, Mr Rajendrasingh G. Yevathikar and Mr Jogendra R. Yadav

The second session of the Seminar was organised in the evening in Atomic Energy Central School No. 2, BARC, Tarapur, for the benefit of the family members of employees. Large number of residents of the colony attended the Seminar.

BARC SCIENTIST HONOURED

◆ Dr S.K. Sikka, Director, Solid State and Spectroscopy Group, BARC, has been chosen to receive the MRSI-ICSC "Superconductivity & Materials Science Annual Prize" for the year 2001. This award will be presented to him during the Annual General Meeting of MRSI to be held at Calcutta during January 31 to February 2, 2001. Dr Sikka works in the area of high pressure physics and shock waves.

◆ Mr Nisar Ahmed Mohammed Siddique Shaikh of Electrical Works Section, Technical Services Division, BARC, has been conferred the award of "Shram Vir" for the year 2000 by the Prime Minister of India.

Mr Nisar Ahmed is a specialist in rewinding and repairing of all types of conventional and special rotating electrical equipments requiring high degree of skill. He has carried out repairs of various critical R&D equipments like micro-motor for dye laser system, special transformer for Nd-YAG laser system, high frequency generator and high voltage high rating motors, etc. On many occasions, Mr Nisar Ahmed has organised major breakdown repair works with minimum time to re-commission various essential utilities in BARC, including devising necessary infrastructure. He has shown exemplary zeal and enthusiasm in discharging his duties thus motivating the other work force.

The award carries a cash prize and a citation.